MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2018/2019

DCS5158 – COMPUTER ARCHITECTURE

(For DIT students only)

18 OCTOBER 2018
09.00 am - 11.00 am
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of **6** pages with **2** sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. The _____ introduced the system software which provides the ability to load programs, move data to peripherals and libraries as well as to perform common computations.

   A. first generation computers
   B. second generation computers
   C. third generation computers
   D. fourth generation computers

2. Which of the following are the main functions performed by a computer?

   I. Data processing
   II. Data storage
   III. Data movement
   IV. Control

   A. I and II
   B. I, II and III
   C. I, III and IV
   D. All of the above

3. Which of the following is the most significant digit of 1908_{10}?

   A. 1
   B. 9
   C. 0
   D. 8

4. What is the value of 101010110.110_2 when converted to decimal representation?

   A. 0.245_{10}
   B. 234.30_{10}
   C. 342.75_{10}
   D. 34.075_{10}

5. Which of the following shows -22_{10} in 8-bit sign-magnitude representation?

   A. $1011\ 0110_2$
   B. $1001\ 0110_2$
   C. $1010\ 1001_2$
   D. $1110\ 0110_2$

Continued...

6. Which of the following instructions is applicable to a special memory organization called a stack?

   A. Three-address
   B. Two-address
   C. One-Address
   D. Zero-address

7. Which of the following are the general categories of data?

   I. Addresses
   II. Numbers
   III. Characters
   IV. Logical data

   A. I, II and III
   B. I, II and IV
   C. II, III and IV
   D. All of the above

8. Based on the mathematical expression x = y + z, which one represents the source of operand?

   A. =
   B. z only
   C. y and z
   D. x and y

9. Which of the following are the common uses of displacement addressing?

   I. Register addressing
   II. Base-register addressing
   III. Indexing
   IV. Relative addressing

   A. I, II and III
   B. I, II and IV
   C. II, III and IV
   D. All of the above

10. Which of the following is **FALSE** about logical operation name and its description?

	Operation Name	**Description**
A.	AND	Perform logical AND
B.	OR	Perform logical OR
C.	Shift	Shift specified condition and set flag
D.	Rotate	Left (right) shift operand , with wraparound end

Continued...

11. A type of memory which is being used to read the data but not to write on it is classified as _____.

A. Random Only Memory
B. Random Access Memory
C. Read Access Memory
D. Read Only Memory

12. A type of ROM that is manufactured without having any initial storage in it is termed as _____.

A. PROM
B. EROM
C. DROM
D. MROM

13. Which of the following is **TRUE** about the address bus?

I. It is used to designate the source or destination of the data on the data bus.
II. If the processor wishes to read a word of data from memory, it puts the address of the desired word on the address lines.
III. The bus width determines the maximum possible memory capacity of the system.
IV. AGP is a type of address bus.

A. I, II and III
B. I, III and IV
C. II, III and IV
D. All of the above

14. The _____ is used for slower peripherals (mice, modems, regular sound cards, low-speed networking) and for compatibility with older devices.

A. processor bus
B. internal bus
C. standard I/O bus
D. backside bus

15. In the following statement, *X* is referring to _____ technique. It is one of the few ways to identify devices.

X is a technique that uses an interrupt service program to poll or ask each I/O module to determine which module caused the interrupt.

A. hardware poll
B. software poll
C. bus arbitration
D. daisy chain

Continued...

16. When the processor, memory and I/O share a common bus, I/O devices can be interfaced with processor in two ways: _____ and _____.

A. memory mapped I/O, direct I/O
B. memory mapped I/O, isolated I/O
C. interrupt-driven I/O, isolated I/O
D. programmed I/O, direct memory access

17. Which of the following is **NOT** an advantage of Direct Memory Access (DMA)?

A. frees CPU
B. higher transfer rate
C. result in cheaper system
D. A and B

18. Which of the following is the **BEST** situation as illustrated in Figure 1?

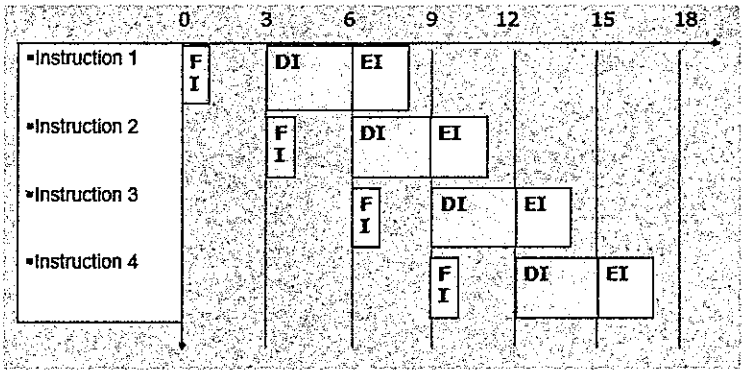

Figure 1

A. Correct timing diagram for unequal stages
B. Latencies are not constant.
C. Stages are executed in parallel
D. Stage delay is too long

19. A _____ occurs when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution.

A. pipeline hazard
B. delayed branch
C. multiple stream
D. delayed control

20. To improve performance, the pipeline should have more _____.

A. memory
B. cycles
C. stages
D. instructions

Continued...

SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer ALL the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 **(20 marks)**

a) List and briefly explain any **FOUR (4)** registers associated with operations performed in the control unit or the ALU. (6 Marks)

b) Show how 25_{10}-37_{10} is calculated in 8-bit binary representation. (7 marks)

c) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert $FC1.1C_{16}$ to a normalized binary value. (2 marks)
ii. Convert 767.121_8 to its hexadecimal equivalent value. (3 marks)
iii. Convert 512.21_8 to a decimal equivalent value. (2 marks)

QUESTION 2 **(20 marks)**

a) Given the following expression,

$$X = [(A + B) * C] - [D * (C + E / L)]$$

i. Convert the expression to postfix notation. (1 mark)
ii. Write the following machine instructions:
- One-address (2.5 marks)
- Two-address (2 marks)
- Three-address (1.5 marks)

iii. Draw the stack diagrams that illustrate the program execution. (3 marks)

b) A computer system has a memory architecture made up of 950MB of main memory and 512KB of cache. In order to perform an efficient mapping function, the main memory is arranged in blocks of 64 bytes. Draw the address structures for the different mapping functions stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping (3.5 marks)
ii. Four-Way Set Associative Mapping (3.5 marks)
iii. Associative Mapping (3 marks)

Continued...

QUESTION 3 (20 marks)

a) Briefly explain **THREE (3)** differences between static RAM and dynamic RAM. (6 marks)

b) Explain the operation of a bus in the computer system. (6 marks)

c) Provide **TWO (2)** reasons on why the PCI bus is the most popular local I/O bus. (2 marks)

d) When the cache is full, the algorithm must choose which items to discard to make room for new ones. List and explain **THREE (3)** most common cache replacement algorithms. (6 marks)

QUESTION 4 (20 marks)

a) Briefly explain the operation of the Interrupt-driven I/O technique. (4 marks)

b) An external device attaches to the computer by a link to an I/O module in the form of control, data and status signals. Briefly explain what is control and status signals with an example for each. (4 marks)

c) State any TWO (2) characteristics of RISC. (2 marks)

d) Given the implementation of non-pipelining and pipelining for **TWENTY (20)** instructions that has **EIGHT (8)** stages pipeline with an equal delay of 0.4 seconds each. Calculate the total processing time, throughput and speedup for the both implementation.

(Note: Please write the appropriate formula) (10 marks)

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